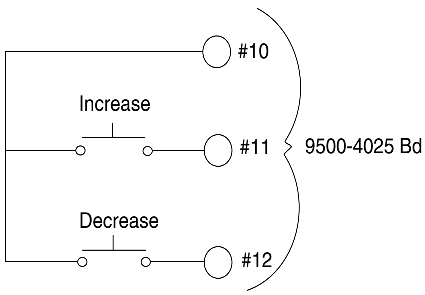
Increase/Decrease MOP Function (with no memory)

The following example utilizes the *Forward/Reverse* input as the increase input and the *Reset* input as the decrease input. If *Forward/Reverse* and *Reset* are required, external relays may be used with the available logic inputs.



Additional Wire Connections

1. Connect terminal #15 to #27 of MDA-2 Bd.
2. Connect terminal #16 to #28 of MDA-2 Bd.
3. Terminal #21 (9500-4025Bd) to #1 (MDA-2 Bd).
4. Terminal #20 (9500-4025Bd) to #3 (MDA-2 Bd).
5. Terminal #19 (9500-4025Bd) to #20 (MDA-2Bd).

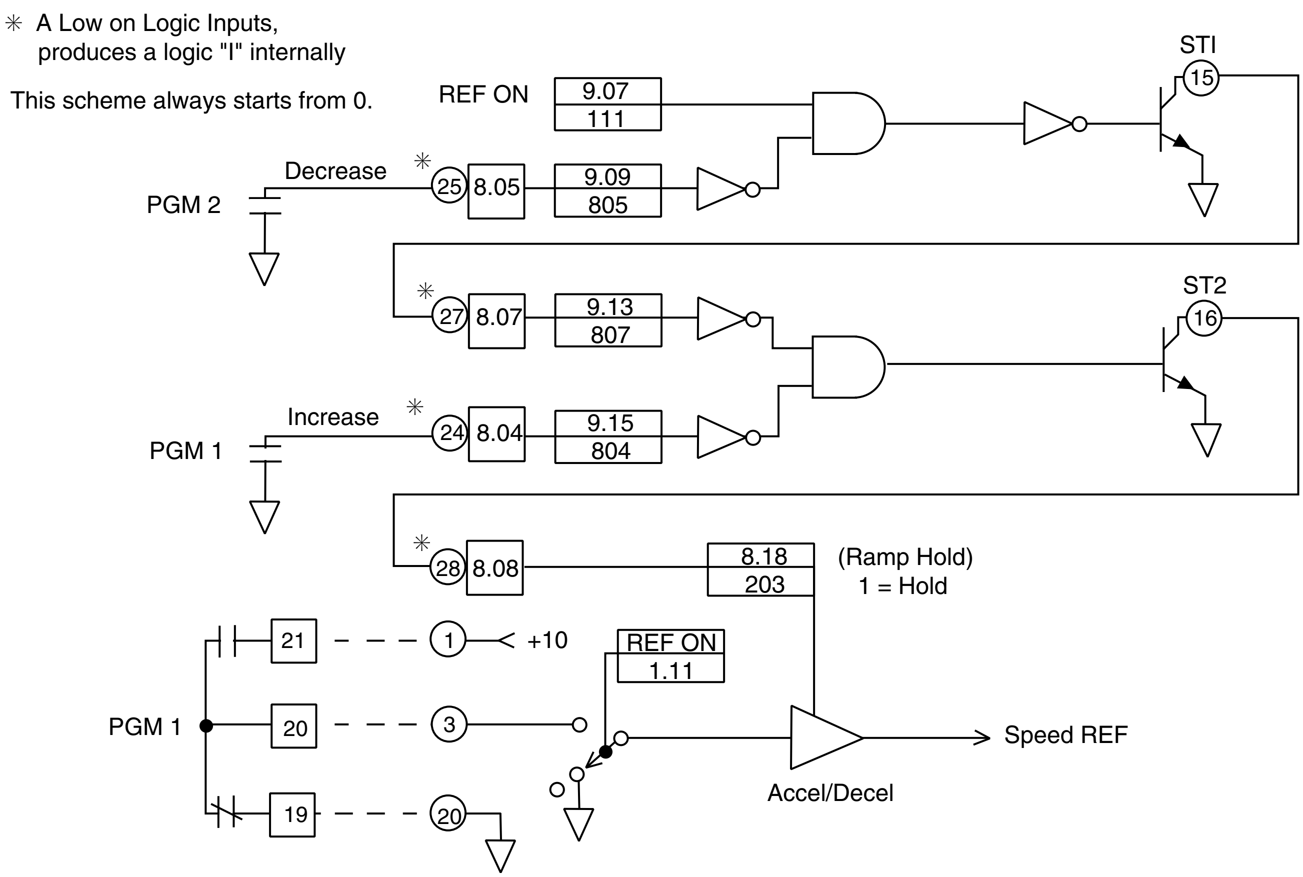
Jumper Program Changes

9500-4030 PC Board — Change jumper JP1 from position 2-3 to position 1-2. This disables *Remote Reset* button to allow it's use as the *Decrease* function.

Program Changes

8.14 = 000
8.15 = 000
8.18 = 203
9.07 = 111
9.08 = 0
9.09 = 805
9.10 = 1
9.11 = 1
9.13 = 807
9.14 = 1
9.15 = 804
9.16 = 1
9.17 = 0

Basic Flow Diagram of Increase/Decrease Logic



Quantum III/Mentor II with Field Boost Transformer

Quantum III/Mentor II with Field Boost Transformer

For 240 VAC applications requiring 240 VDC armature and 240 VDC field voltage.

V_{FLD} (max) = .9 [V_{PRI} + V_{sec}]

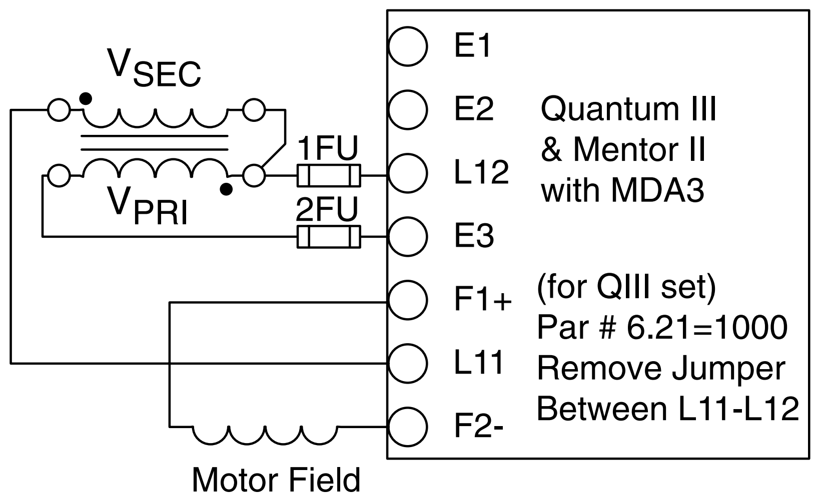
V_{PRI} = Supplied Line Voltage

$VA_{(T1)} = 1.5 \times I_F \times V_{SEC}$

$V_{SEC} = \frac{V_{FLD}}{0.9} - V_{pri}$

NOTES:

1. Transformer T1 can be either an Isolation Transformer as shown or an Auto Transformer.
2. E1 and E3 must also be connected to L1 and L3 respectively as per the User Guide.
3. Fuse 1FU should be sized to protect the secondary winding. Fuse 2 FU should be sized to protect the primary winding



Quantum III *Zero Reference Start Circuit Interlock*

I.Two Wire Control

Parameter Changes:

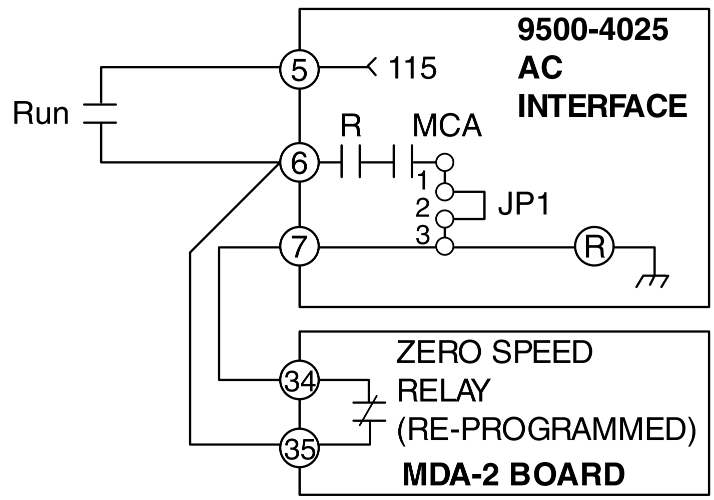
	PR 9.25	=	1201
	PR 12.03	=	705
*	PR 12.04	=	015

* This parameter set % of reference where "zero speed" relay is energized.

Description of Operation:

The zero speed relay has been reprogrammed to energize when the speed pot reference (or external reference into Terminal #3 on the MDA-2 Board) is greater than 1.5% of full speed. The state of this relay as shown above is a closed connection when the reference is less than 1.5%. If the run contact is closed, the drive will start since the "zero speed" contact is closed. Once the contactor picks-up, this zero speed contact is "sealed-in" by the Run (R) an Motor Contactor Auxiliary (MCA) contacts.

If the speed pot is set greater than 1.5%, the drive will not start since the "zero speed" relay contact is open.



II. Three Wire Control

Parameter Changes:

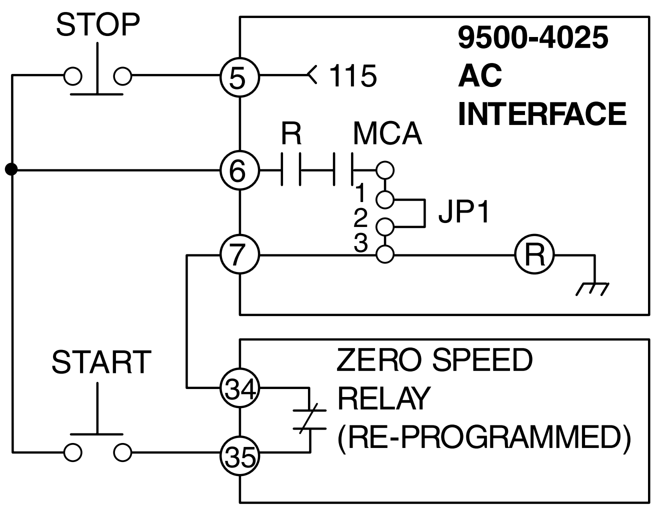
	PR 9.25	=	1201
	PR 12.03	=	705
*	PR 12.04	=	015

* This parameter set % of reference where "zero speed" relay is energized.

Description of Operation:

The zero speed relay contact has been reprogrammed to energize when the speed pot reference (or external voltage reference into terminal #3 on the MDA-2 Board) is greater than 1.5%.

This contact "blocks" the start button until the speed pot reference is set to less than 1.5%. Once the drive is started, the circuit is "sealed-on".



Quantum III *E-Stop without External Trip*

E-Stop without External Trip

In some applications it is desirable to have two stop modes:

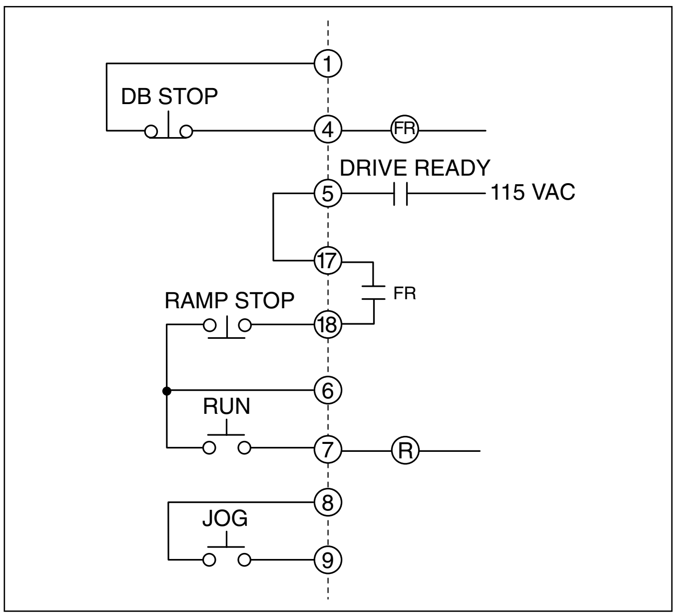
(1) Ramp Stop

(2) Dynamic Braking Stop

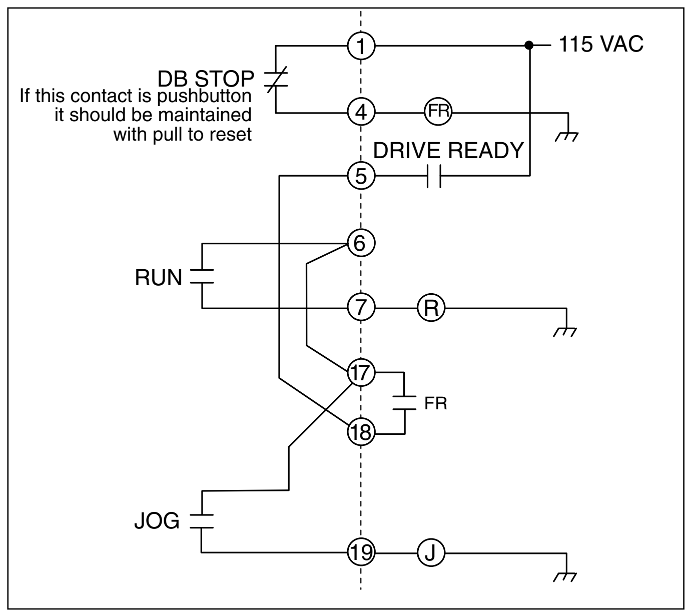
The Quantum III is capable of both type stops in it's standard default configuration with the exception that when a dynamic braking stop command is given (via E-Stop), the drive will fault on Et (External trip). In order to re-start the drive the reset pushbutton must be depressed to reset the fault. In some systems this may not be desirable.

The drive may be reconfigured such that an "Et" fault does not occur with a DB (Dynamic Braking) stop.

Three Wire Run/Stop Pushbuttons



Two Wire Control Run/Ramp Stop + DB Stop



Step 1)

JP3 on 9500-4030 board (Upper interface board)

Pos. 2-3

Step 2)

Change Parameter # 8.16 = 5.17

Press Reset

Set # XX.00 = 1

Press Reset

Step 1) 9500-4030 board (Upper interface board)

JP3 = Pos. 2-3

Step 2) 9500-4025 board (Lower relay board)

JP1 = Pos. 1-2 (see 8.11.1)

Step 3) Change Parameter # 8.16 = 5.17

Press Reset

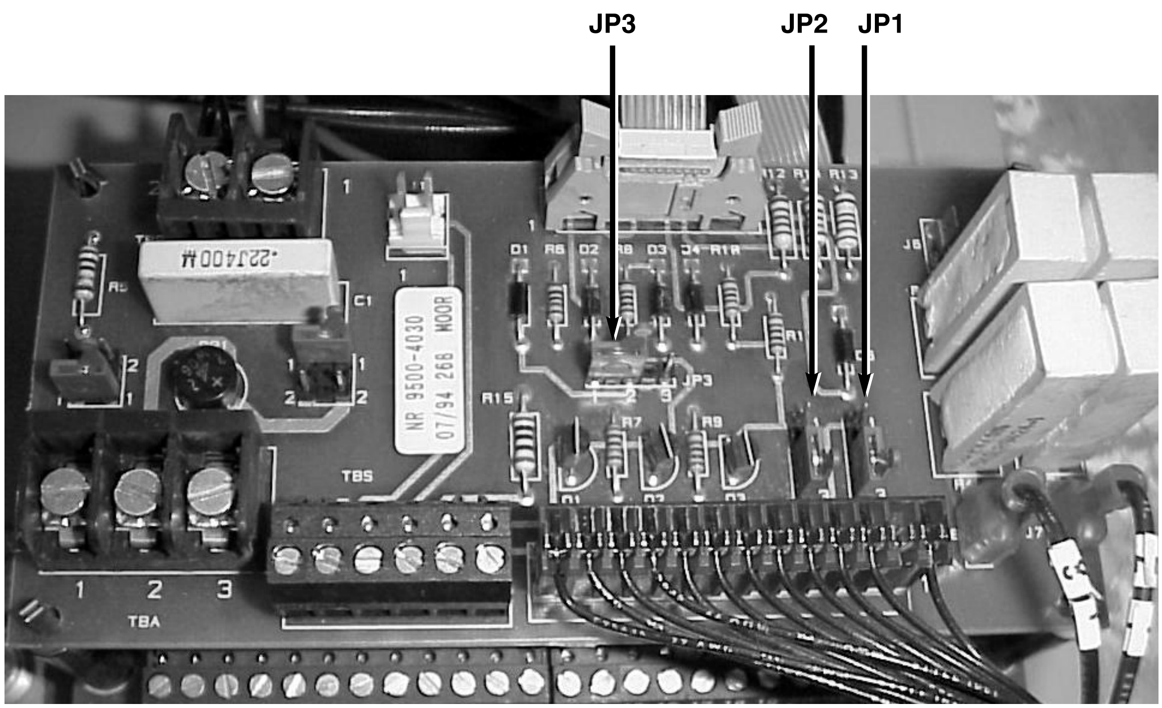
XX.00 = 1

Press Reset

Other Jumper Selections on 9500-4030 Interface Board

JP1	Selection to determine the meaning of 115 VAC Programmable Input #2 (TB1 Pin 12)		
	Position	1-2	Select Digital Reference #3 (Parameter #1.19) as the Speed Reference i.e. for Thread or Drool Speed
	Position	**2-3**	**Remote Drive Reset**
JP2	Selection to determine the meaning of the FR (Fault Relay) Output (TB1 Pins 17 & 18)		
	Position	1-2	External Trip Inactive. FR Relay output contacts usable
	Position	**2-3**	**Loss of 115 VAC from TB1 Pin 4 will cause External Trip**
JP3	Selection to determine how the Drive is to stop		
	Position	**1-2**	**COAST STOP (Armature Contactor Opens upon STOP input)**
	Position	2-3	RAMP STOP (Reference is ramped to zero then Armature Contactor Opens)

Items in **bold** are factory settings.



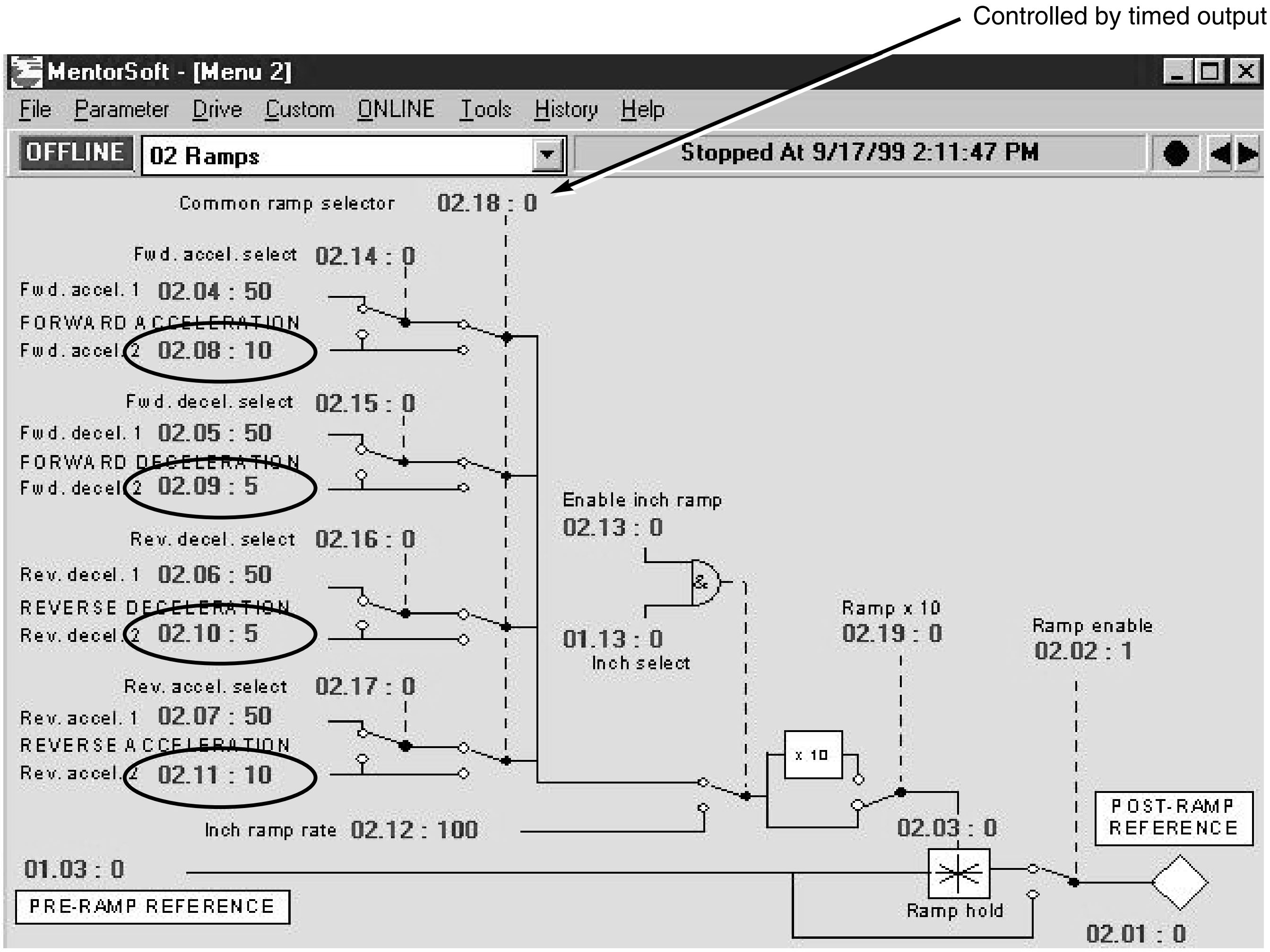
Separate Jog Accel & Decel Ramps

When using the jog function to index a machine into position, it is often desirable to have a smooth accel and quick decel control once the desired position is reached. The Quantum III has a myriad of accel and decel rates for a run reference but has only one overall Jog Accel/Decel rate. If you need a separate Jog Accel and a Jog Decel rate the following configuration changes can provide you with this functionality. This scheme uses set #2 of the Run Accel/ Decel Rates during the Jog period instead of the singular Jog Rate. The time delay programmed by parameter #9.12 maintains the selection of these rates for 2 seconds after the Jog command is removed. Otherwise the rate selector would switch to Accel/Decel set #1. This time can be adjusted to accommodate jog decel rates greater than 2 seconds. This delay just needs to be slightly greater than the Jog decel rate set into #2.09 or #2.11.

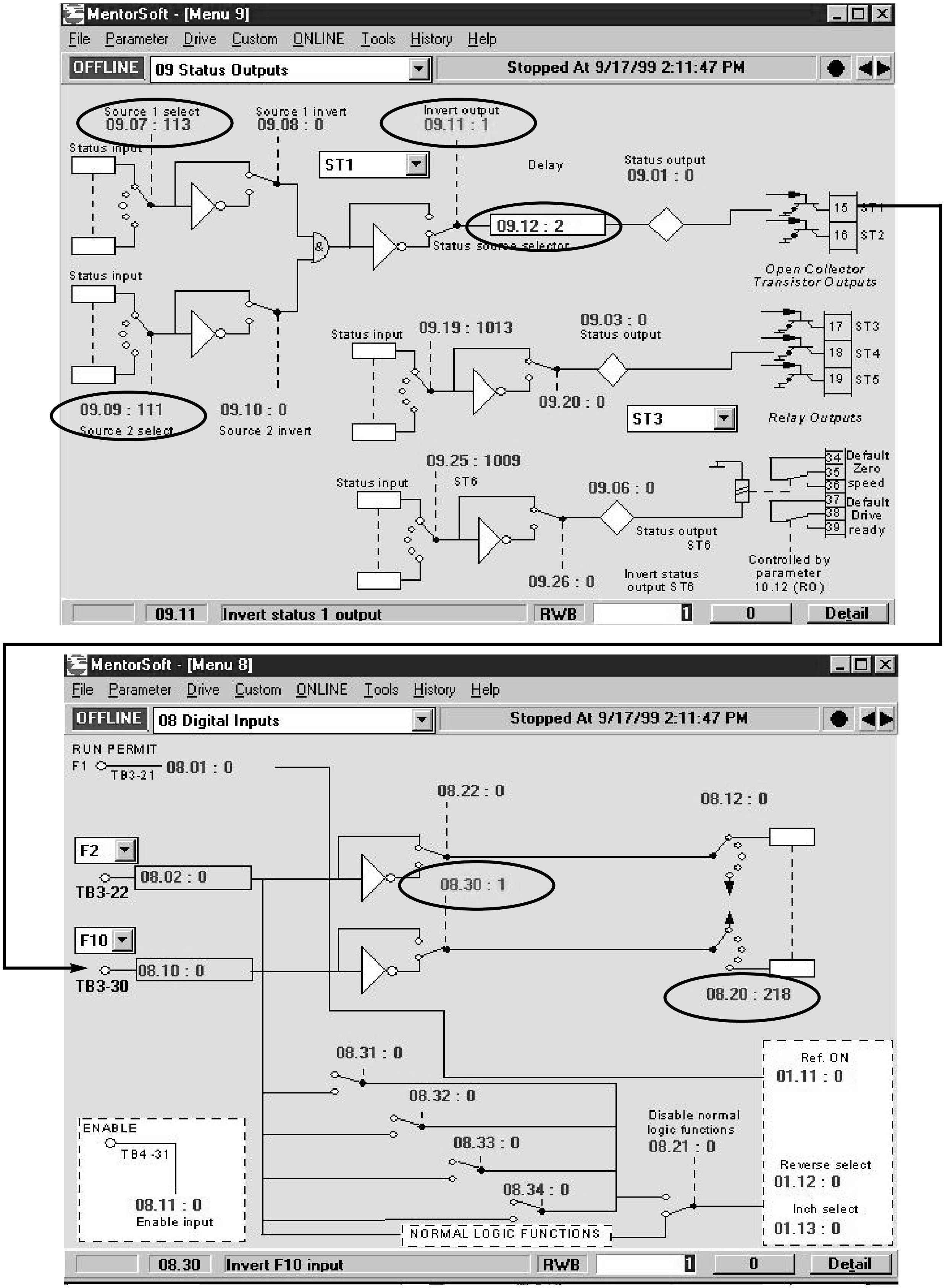
Separate Jog Accel and Decel Rates

PARAMETER NUMBER	CHANGE VALUE TO:	NOTES
2.08	1-1999	Set to Desired Jog Fwd Accel Ramp Rate ie. 10=1 second
2.09	1-1999	Set to Desired Jog Fwd Decel Ramp Rate ie. 5=0.5 seconds
2.10	1-1999 *	Set to Desired Jog Rev Accel Ramp Rate ie. 10=1 second
2.11	1-1999 *	Set to Desired Jog Rev Decel Ramp Rate ie. 5=0.5 seconds
2.13	0	Disable the Normal Jog Ramp Rate
8.20	218	Direct this result to Run Accel/Decel Rates Bank Selector
8.30	1	Invert F10 Input (TB3-30)
9.07	113	Look at the Jog Command with AND gate input #1
9.09	111	Look at the Drive Ref On with AND gate input #2
9.11	1	Invert this result
9.12	2	Sustain this result for 2 seconds following a Jog command
Install a Jumper wire between TB2-15 (ST1 Logic Resultant) and TB3-30 (F10 input) on the MDA2 or MDA2B interface board terminal strip.		
* Reverse assumes use with a Regen Drive Model.		
Note: Fast Jog Deceleration implies the use of a Regen Drive Model. With Non-Regenerative models the decel rate is a function of the machine load/friction. If a fast jog decel is needed in this instance, perhaps the application of Dynamic Braking could be utilized.		

Separate Jog Accel and Decel Rates (continued)



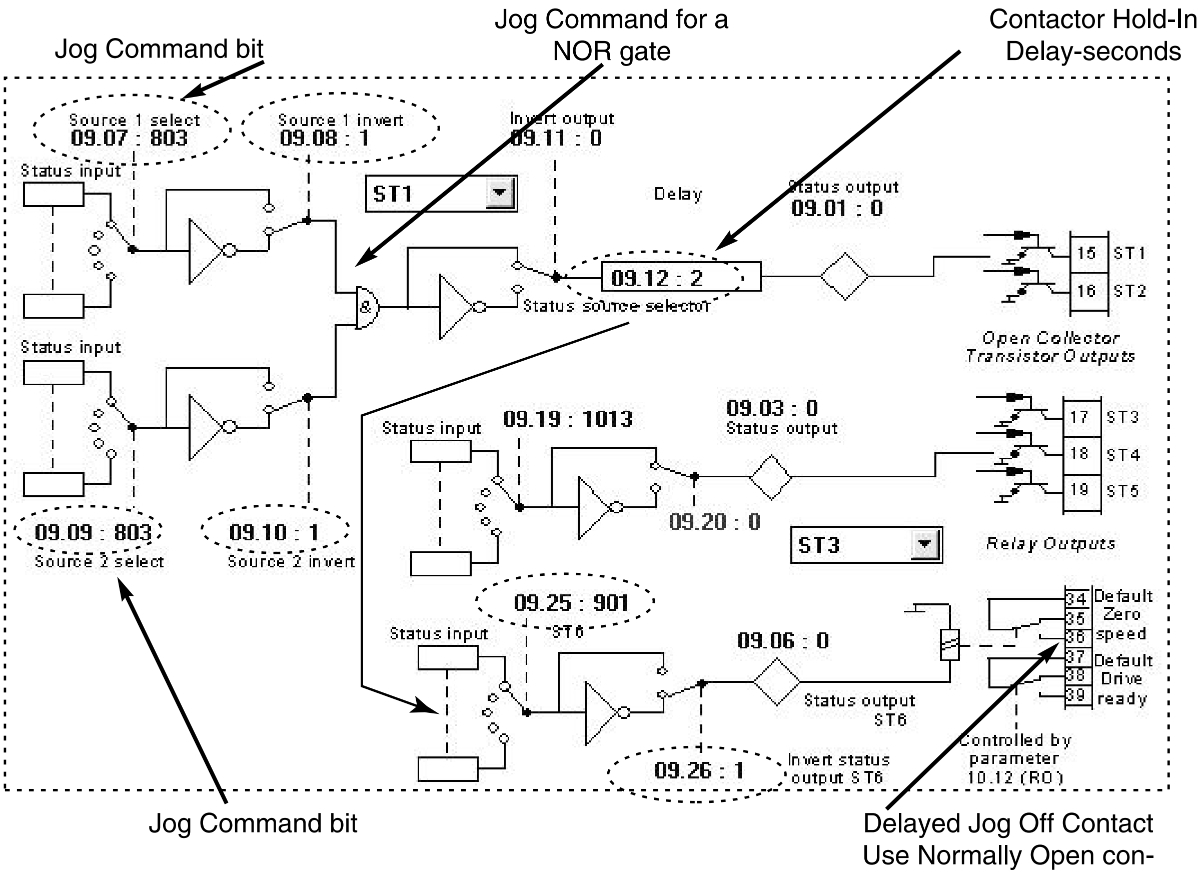
Separate Jog Accel and Decel Rates (continued)



"Contactor-Less" Jog
Delayed Motor Contactor Hold-In

When jogging, the "banging" of the contactor on Quantum III can be rather annoying not to mention causing things on the panel to vibrate loose and also tends to accelerate general wear and tear on this electromechanical device. It is often desirable to hold the contactor "in" for a couple of seconds after a jog (anticipating more jogging) then "dropping out" the motor contactor. This can provide a "contactorless" jog feel and reduce the effects mentioned above.

This application note illustrates how to utilize the "built-in" logic function and time-delay blocks to embellish the Jog function provided in the Quantum III.



To complete this Quantum III application one would make the following wiring connections:

FROM	TO
pin 34 of TB3 on the MDA2B board	pin 13 of the AC Interface Board
pin 36 of TB3 on the MDA2B board	pin 24 of the AC Interface Board
pin 14 of the AC Interface Board	pin 5 of the AC Interface Board

These connections will provide a method for this delayed off contact to hold in the contactor but only after the contactor has been picked up by an initial Jog request. (The RUN/JOG contact, TB13-14 on the AC Interface board, is used as a permissive for the delayed contact created above).

A similar approach could be used for a Mentor II but one would need to make the necessary translations. (Jog F and Jog R would be the inputs to the NOR gate).

In practice, this Jog Hold-In scheme may not be effective with non-regenerative models (9500-83xx) on machine loads with low friction and higher inertia or loads that tend to coast for a while. For this reason, this scheme is probably most effective with regenerative models.

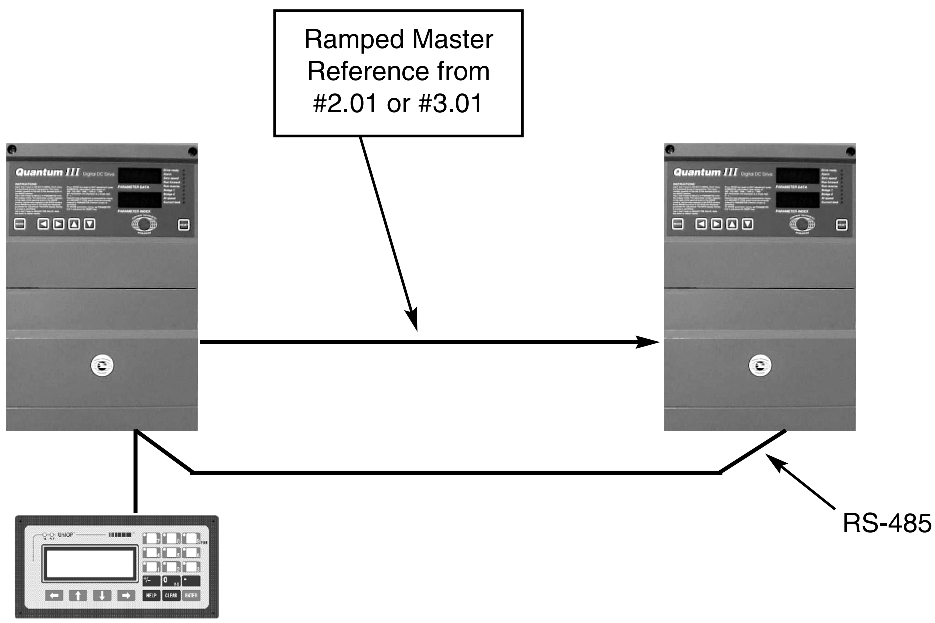
A Simple Ratio Control Scheme

I've been asked on a couple of occasions about

"How could one achieve simple ratio control without encoder feedback and without the MD-29 and associated programming costs?"

The User in these cases did not need or want digital lock nor want to upgrade from DC tachs but would like to give the Operator digital control of ratio.

With the UniOp, the Line Speed setpoint could be directly entered by the Operator or trimmed with Up/Down arrows. The Ratio could be directly entered by the Operator or trimmed with Up/Down arrows also. By using the UniOp, Fault Messages, general Drive Info such Arm V, Arm Amps, %Load, Motor RPM etc could also be brought to the User in simple terms as well.



Line Speed=1000FPM ← **-Reads #3.02 of Master**
FPM Setpoint=1000FPM ← **-Writes to #1.18 of Master**
Draw Ratio=1.234 ← **-Writes to analog input scaling parameter**
Draw Roll = 1234FPM ← **-Reads #3.02 of slave**

For more Application Notes visit our website at:
www.ctdrives.com/downloads under Application Notes.

Programmable Logic Gates

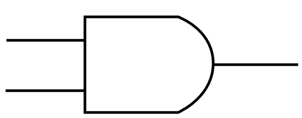
The following discussion hopefully will help to understand and use these useful programmable logic functions a little better.

There are 2 sets of dual input logic gates within the Unidrive and Quantum/Mentor drive intended to help with miscellaneous system logic. The fundamental building block of these gates use the AND gate. By placing selectable inverters before each input to the AND gate and an inverter after the AND gate, all four logic functions namely AND, NAND, OR and NOR can be achieved. Since there are 2 of these gates in each drive, 3 input AND, NAND, OR and NOR gates can also be achieved.

The AND gate

The AND gate is the simplest of the logic functions to realize. For this to be accomplished, one would simply not use the input or output inverters on this logic function. The boolean equation for AND is Y= A•B or Y= AB (both read as Y= A and B).

Input A	Input B	Output Y
0	0	0
0	1	0
1	0	0
1	1	1



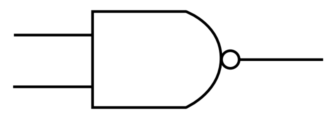
The NAND gate

The NAND gate is also easy to realize. The NAND is simply NOT AND or the inverse of AND. One would simply use the output inverter on this logic function to achieve the NAND function.

The boolean equation for NAND is:

Y=A•B or Y= AB (both read as Y= A and B not).

Input A	Input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0



The NOR gate

The NOR function is not as intuitive to realize. The secret lies in knowing the alternate symbology for various gates. The boolean equation for NOR function is:

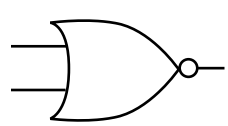
Y= A+B   (read as Y= A or B not).

DeMorgan's theorem states that the equivalent logic function can be realized removing the "overall inversion bar" by changing the OR operator to AND plus inverting the variables thus becoming

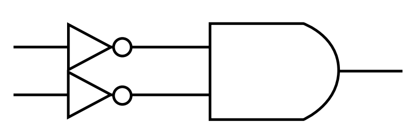
Y= A•B   (read as Y = A not AND B not).

Therefore we can easily achieve the NOR function on the drive logic functions by inverting the inputs before the AND gate.

Input A	Input B	Output Y
0	0	1
0 1	0	
1 0	0	
1 1	0	



NOR symbol

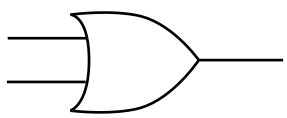


Equivalent NOR symbol

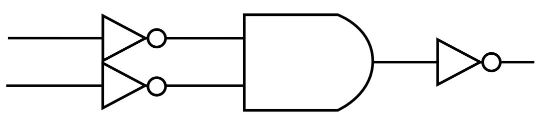
The OR gate

Once we have a NOR gate the OR function is easy- we simply invert the NOR using the inverter on the output of the logic function block.

Input A	Input B	Output Y
0	0	0
0	1	1
1	0	1
1	1	1



OR symbol



Equivalent OR symbol

In Summary, the tables listed below should help one achieve the desired logic gates using the drives programmable logic functions.

FOR QUANTUM III

Gate #1

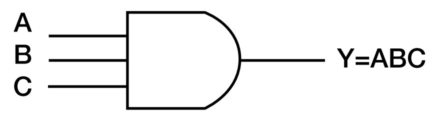
LOGIC GATE TYPE	INPUT #1 INVERTER #9.08	INPUT #2 INVERTER #9.10	OUTPUT INVERTER #9.11	FINAL GATE OUTPUT #9.01
AND	0	0	0	
OR	1	1	1	
NAND	0	0	1	
NOR	1	1	0	

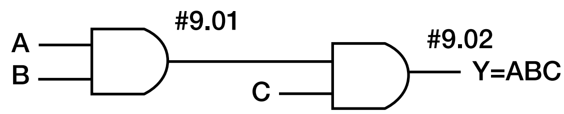
Gate #2

LOGIC GATE TYPE	INPUT #1 INVERTER #9.14	INPUT #2 INVERTER #9.16	OUTPUT INVERTER #9.17	FINAL GATE OUTPUT #9.02
AND	0	0	0	
OR	1	1	1	
NAND	0	0	1	
NOR	1	1	0	

3-Input Gates

By virtue of having 2 two input logic gate functions, 3 input gates can be achieved. For example, to achieve a 3 input AND function, one would simply use logic gate #1 to perform the first AND and then obtain this result from the second AND gates input source then AND that with the remaining input of the second AND gate.



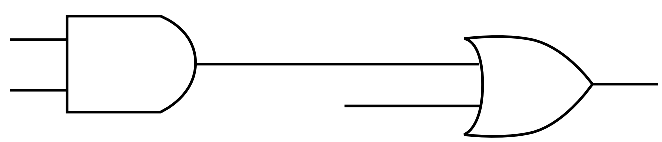


Obviously, this same procedure would be used to obtain the other types of 3 input gates (NAND, OR, NAND).

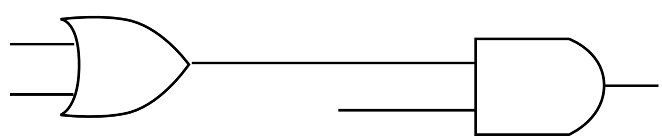
Combinational Logic

Using similar techniques as described above, the standard AND/OR and OR/AND function can be obtained to provide logic functions such as those shown below.

AND/OR **Y= (A•B) + C**



OR/AND **Y= (A+B) • C**



Naturally, various renditions of these can be achieved through use of the input and output inverters to arrive at functions such as:

Y= (A•B) + C

Y= (A+B) • C

Quantum III *Programmable Time Delays*

Built-in to Quantum III product are two sets of Programmable Logic Gates. In addition, each logic gate has a programmable time delay output. This article was created to promote the understanding and application of these built-in Time delays.

For additional info one could refer to Menu 9 block diagrams for these drives.

The output delay functions will produce an output with a logic "high" input after the time delay setting. For Quantum III these delays can range form 0-255 seconds.

Figure 1 illustrates the time delay action basic on the logic high input. Note that transitions of "high to low" are immediate.

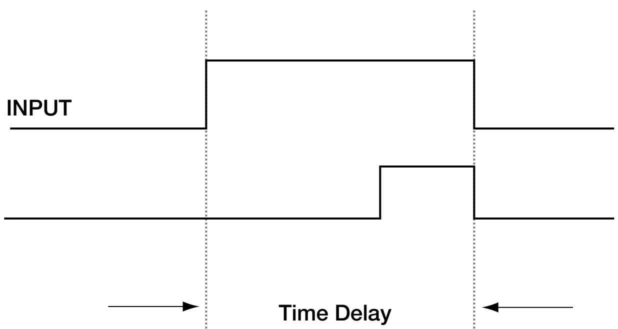


Figure 1.

Figure 2 illustrates that input transitions shorter than the time delay will be "masked". This could have application in "debouncing" a comparator (without hystersis) that is just hovering past a threshold setting.

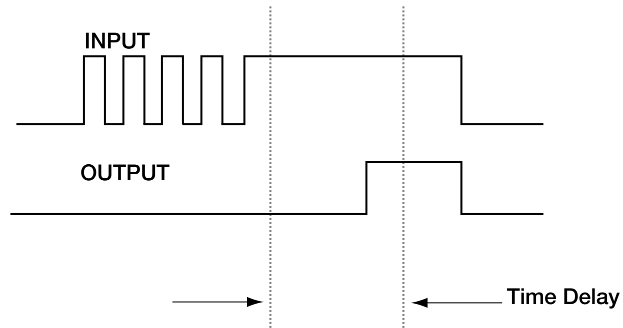


Figure 2.

For a practical example of how one might use the logic gates with time delay, suppose you had a need to know if the motor was in a "stalled condition". The criteria for this determination might be:

STALLED = AT ZERO SPEED * IN CURRENT LIMIT

or

STALLED = AT ZERO SPEED * CURRENT> SOME AMOUNT

In either case, during a quick start the Drive would be At Zero Speed and delivering a high current. A simple **AND** might create a momentary output at start. So this calls for the AND condition to exist for perhaps 3 seconds before we've reached the conclusion that the motor is indeed STALLED. This is where the Time Delay function could come into play.

For more Application Notes visit our website at:

www.ctdrives.com/downloads under Application Notes.